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YOR920000173US2

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	6,143,582	11/07/2000	Vu et al.			
	6,346,446	02/12/2002	Ritenour			
	6,365,465	04/02/2002	Chan et al.			

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	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO

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	"Self-Aligned (Top and Bottom) Double-Gate MOSFET with a 25 nm Thick Silicon Channel", Hon-Sum Philip Wong, Kevin K. Chan, and Yuan Taur, IBM Thomas J. Watson Research Center, Yorktown Heights, NY, IEEE 1997, pp. 427-430
	"New Planar Self-Aligned Double-Gate Fully-Depleted P-MOSFET's Using Epitaxial Lateral Overgrowth (ELO) and Selectively Grown Source/Drain (S/D), Taichi Su, John P. Denton, and Gerold W. Neudeck, IEEE School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN, IEEE, 2000, pp. 110-111

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	"0.18-um Fully-Depleted Silicon-on-Insulator MOSFET's", Min Cao, Ted Kamins, Paul Vande Voorde, Carlos Diaz, and Wayne Greene, IEEE Electron Device Letters, Vol. 18, No. 6, June 1997, pp.251-252
	"Super Self-Aligned Double-Gate (SSDG) MOSFET's Utilizing Oxidation Rate Difference and Selective Epitaxy", Jong-Ho Lee, Gianni Taraschi, Andy Wei, Tom A. Langdo, Eugene A. Fitzgerald, and Dimitri A. Antoniadis, Microsystems Technology Laboratories, Massachusetts Institute of Technology, Cambridge, MA, IEEE, 1999, pp71-74

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